Disclosur Stat m nt dated September 17, 1999, and to provid a dated, initialed copy of the Information Disclosure Citation form as evidence that the document has been considered and will be cited of record.

An Information Disclosure Statement was also filed on October 20, 2000, whereby the Doan et al. reference (U.S. Patent No. 5,946,595) was submitted. However, the Examiner has not acknowledged receipt of the Information Statement dated October 20, 2000. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement dated October 20, 2000, and to provide a dated, initialed copy of the corresponding Information Disclosure Citation form as evidence that the document will be cited of record in the present application.**

Also, an Information Disclosure Statement was recently filed on May 1, 2001, whereby the Besser et al. reference (U.S. Patent No. 6,165,903) was submitted. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement dated May 1, 2001, and to provide an initialed, dated copy of the Information Disclosure Citation form as evidence that the document has been considered and will be cited of record in the present application.**

Specification

The Examiner has requested identification of the parent application via amendment of the present divisional application. The Examiner is however respectfully

directed to the Preliminary Amendment filed along with the present application on September 17, 1999, whereby the specification was amended to make reference to parent application serial no. 09/342,751.

Claim Rejections-35 U.S.C. 112

Claim 22 has been rejected under 35 U.S.C. 112, second paragraph as being indefinite. The Examiner has asserted that "said providing a field oxide layer and an SOI layer" is indefinite. However, clear antecedent basis for this feature may be found in independent claim 9. Thus, it is unclear how this language may be considered indefinite. The Examiner is therefore respectfully requested to withdraw this aspect of the rejection.

The Examiner has further asserted that claim 22, lines 3-5 are indefinite in that it is not clear what the expression means. However, on page 4 of the Final Office Action dated February 13, 2001, the Examiner has acknowledged that the corresponding language has been interpreted to mean that the first-reacted silicide regions are completely formed and that silicon remains after the second RTA process. This interpretation may be considered as a correct interpretation. Thus, it is apparent that the above noted expression is clear, definite and understandable.

With regard to the language "so that an appropriate amount of the silicon remains in the SOI layer", the Examiner is respectfully directed to Manual of Patent Examining Procedures section 2173.05(c) III, which points out that in more recent

cases, features such as "an effective amount" (or as in this case "an appropriate amount") are definite when read in light of the supporting disclosure and in the absence of any prior art which would give rise to uncertainty about the scope of the claim. Applicant respectfully submits that the "appropriate amount" of claim 22 is definite when read in light of the supporting disclosure of the present application, particularly in view of the Examiner's specific acknowledgment on page 4 of the present application regarding these features. Accordingly, the Examiner is respectfully requested to reconsider and withdraw this corresponding rejection for at least the above reasons.

Claim Rejections-35 U.S.C. 103

Claims 1-9 and 19-20 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of the Doan et al. reference (U.S. Patent No. 5,946,595). This rejection is respectfully traversed for the following reasons.

As described with respect to prior art Figs. 1A-1C on page 7 of the present application, after the first rapid thermal annealing (RTA) process, the remaining Co and TiN metal layers are removed. Thereafter, the second RTA process is carried out so that silicon in SOI layer 18 and in poly-silicon gate layer 22 again react with silicide regions 30 and 32. The silicide regions 30 and 32 thus become $CoSi_2$, which has lower resistance. However, if SOI layer 18 of the prior art device is formed to have irregular thickness, thinner parts of SOI layer 18 may be silicided entirely, such that voids may

be formed in SOI layer 18. In extreme instances, buried oxide layer (BOX) 14 may be etched when contact holes are formed in the active area, and silicon substrate 12 may also be etched.

In order to overcome these problems of the conventional fabrication processes, in a preferred embodiment of the present application polysilicon layer 136 is formed over the entire structure as a supplemental silicon layer, prior to the second RTA process. As may be readily understood in view of Figs. 2D and 2E, supplemental silicon layer 136 is formed subsequent to removal of Co layer 126 and TiN layer 128, and after the first RTA process. **In this manner, silicon for the silicide process during the second RTA process is provided not only from SOI layer 118 and poly-silicon gate layer 122, but also from supplemental silicon layer 136.** Accordingly, the first-reacted silicide regions 130 and 132 respectively formed in SOI layer 118 and in polysilicon gate layer 122, may be converted respectively into second-reacted silicide regions 138 and 140 having lower resistance, as illustrated in Fig. 2E. In view of the supplemental silicon layer, enough silicon remains in SOI layer 118 after the second RTA process, so that BOX layer 114 is prevented from being etched.

The method of fabricating a semiconductor device of claim 1 includes in combination "performing a first RTA (Rapid Thermal Annealing) process to form a first-reacted silicide region"; "providing a supplemental silicon layer over the surface of the semiconductor device, including the first-reacted silicide region" and "performing a second RTA process to convert the first-reacted silicide region into a second-reacted

silicide region, by reaction of the supplemental silicon layer with the first-reacted silicide region". Applicant respectfully submits that the prior art as relied upon by the Examiner does not make obvious these features.

As emphasized above, the prior art as described with respect to Figs. 1A-1C of the present application is not disclosed or suggested as providing a supplemental silicon layer over the structure, particularly prior to performing a second RTA process. The Examiner has relied upon the Doan et al. reference and has interpreted polysilicon layer 24 of Figs. 3-5 for example, as the supplemental silicon layer of claim 1. However, Applicant respectfully submits that one of ordinary skill would have no motivation to modify prior art Figs. 1A-1C of the present application to include polysilicon layer 24 of the Doan et al. reference as a supplemental silicon layer.

Particularly, polysilicon layer 24 is used in the Doan et al. reference for the purpose of forming local interconnects. Polysilicon layer 24 is formed directly on titanium layer 22. Polysilicon layer 24 is selectively etched as illustrated in Fig. 5, and is subsequently subjected to an RTA process as illustrated in Figs. 6 and 7, so that the portions of titanium layer 22 which are covered by polysilicon layer 24 are converted into regions of titanium silicide 28. These patterned regions of titanium silicide 28 serve as titanium salicide local interconnects.

Thus, in the Doan et al. reference, polysilicon layer 24 is converted into an interconnect, and is not used as a supplemental silicon layer, as in claim 1. Particularly, polysilicon layer 24 of the Doan et al. reference is formed **on titanium layer 22, and**

thus r acts with titanium lay r 22 during the RTA proc ss. Polysilicon layer 24 does not react with a first-reacted silicide region of a semiconductor substrate, to convert the first-reacted silicide region into a second-reacted silicide region, as in claim 1.

Applicant emphasizes that one of ordinary skill would have no motivation to modify the process of prior art Figs. 1A-1C of the present application in view of the Doan et al. reference, to arrive at the method of fabricating semiconductor device of claim 1. The Doan et al. reference would suggest forming a polysilicon layer on TiN layer 28 of Fig. 1B of the present application, and performing an RTA process to transform the polysilicon layer and TiN layer 28 into a titanium silicide interconnect. The Doan et al. reference fails to suggest providing a supplemental silicon layer **over a first-reacted silicide region**, and subsequently performing an RTA process **to convert the first-reacted silicide region into a second-reacted silicide region**, "by reaction of the supplemental silicon layer with the first-reacted silicide region", as in claim 1. Accordingly, Applicant respectfully submits that the method of fabricating semiconductor device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that the rejection of claims 1-8 and 19-21 is improper for at least these reasons.

Applicant respectfully submits that the method for fabricating a semiconductor device of claim 9 would not have been obvious in view of the prior art as relied upon by the Examiner for at least similar reasons as set forth above with respect to claim 1.

Particularly, the Doan et al. reference as relied upon by the Examiner would not motivate one of ordinary skill to modify prior art Figs. 1A-1C of the present application to remove non-reacted material from a first-reacted silicide region, to provide a supplemental silicon layer over the surface of the semiconductor device after the non-reacted material is removed, and to perform a second RTA process to convert the first-reacted silicide regions into second-reacted silicide regions, by reaction of the supplemental silicon layer with the first-reacted silicide regions. Polysilicon layer 24 of the Doan et al. reference does not react with first-reacted silicide regions that are formed in a polysilicon gate layer and in source/drain active areas of an SOI layer. Polysilicon layer 24 merely reacts with titanium layer 22 to form titanium silicide interconnects 28. Applicant therefore respectfully submits that the method for fabricating a semiconductor device of claim 9 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and the rejection of claims 9 and 22 is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections and to pass the claims of the present application to issue for at least the above reasons.

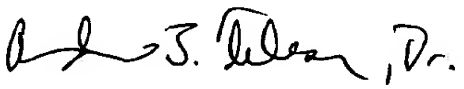
In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581)

at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

JONES VOLENTINE, P.L.L.C.



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